

VDIC EEPROM MEMORY

VDEE8M08XS40XX8V250-II USER MANUAL

Version : A0

Document NO.: ORBITA/SIP-VDEE8M08XS40XX8V250-II-USM-01

Zhuhai Orbita Aerospace Science & Technology Co. , Ltd.

Add: Orbita Tech Park, NO.1 Baisha Road, Tangjia Dong ` an,

Zhuhai, Guangdong, China 519080

Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

1	DESCRIPTION	1
2	FEATURES	1
3	BLOCK DIAGRAM	2
4	PIN DESCRIPTIONS	2
5	COMMAND OPERATION	3
5.1	ABSOLUTE MAXIMUM RATINGS	3
5.2	RECOMMENDED DC OPERATING CONDITIONS.....	4
5.3	DC CHARACTERISTICS ($V_{CC}=2.7\text{ V}$ TO 3.6 V).....	4
6	TYPICAL APPLICATION	4
7	ORDERING INFORMATION.....	5
8	PACKAGE DIMENSIONS.....	6
9	REVISION HISTORY	7

VDIC-EEPROM

3.3V 1M×8bit

1 Description

The VDEE8M08XS40XX8V250-II is a 1M×8bit Electrically Erasable and Programmable CMOS ROM. It is organized as eight dies of 1Mbit. Each die has 8-bit interface and is selected with specific #CE. All other signals are common to the eight EEPROM 1Mbit. The device is manufactured using well known SIP technology. It is particularly well suited for use in high reliability, high performance and high density system applications.

The VDEE8M08XS40XX8V250-II is packaged in a 40 pins SOP.

2 Features

- Single 3.3V Power supply: 2.7 V to 3.6V
- Access time: 250 ns (max)
- Power dissipation
 - Active: 160 mW/MHz, (typ)
 - Standby: 880 μW (max)
- On-chip latches: address, data, #CE, #OE, #WE
- Automatic byte write: 10 ms (max)
- Automatic page write (128 bytes): 10 ms (max)
- Data polling and RDY/#Busy
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10⁴erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by #RES pin

3 Block Diagram

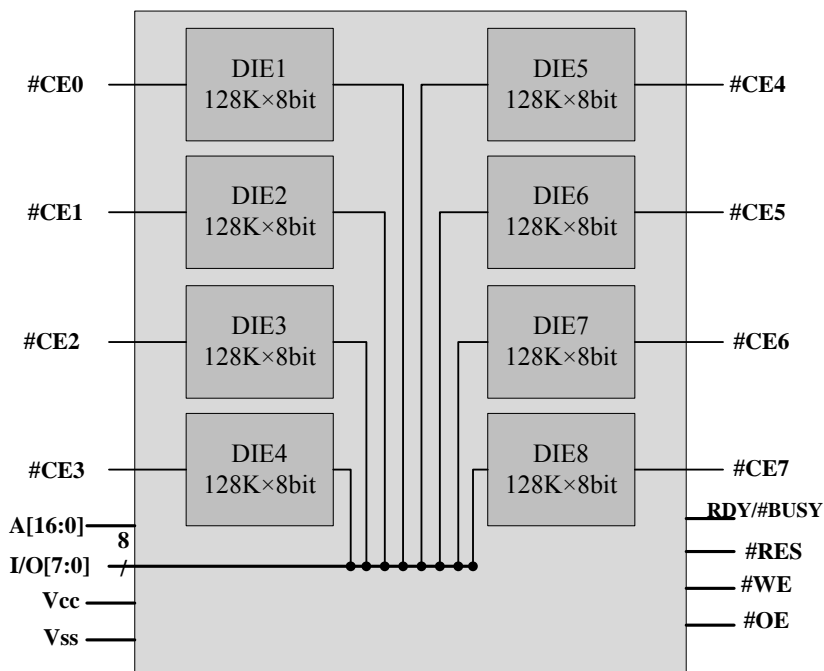


Figure 1 Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
VSS	1	40	#CE2
#CE7	2	39	#CE1
A11	3	38	#OE
A9	4	37	A10
A8	5	36	#CE0
A13	6	35	I/O7
#WE	7	34	I/O6
#RES	8	33	I/O5
A15	9	32	I/O4
VCC	10	31	I/O3
RDY/#BUSY	11	30	VSS
A16	12	29	I/O2
A14	13	28	I/O1
A12	14	27	I/O0
A7	15	26	A0
A6	16	25	A1
A5	17	24	A2
A4	18	23	A3
#CE5	19	22	#CE3
#CE6	20	21	#CE4

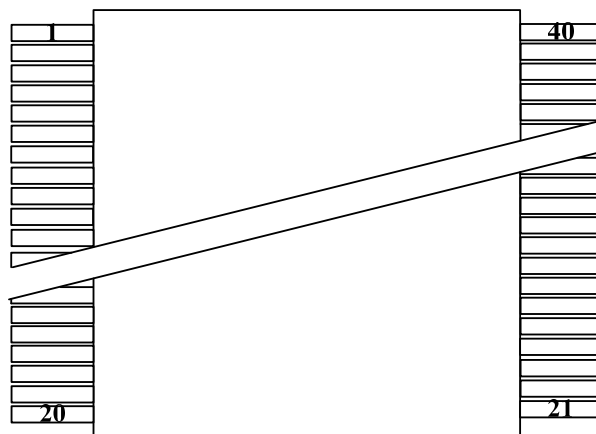


Figure 2 Pin configuration

Table 1 Pin description

Name	Function
A0~A16	Address Input..
I/O0- I/O7	Data Input/Output Ports. 8 bi-directional ports are used to read data from or write data into the EEPROM.
#CE0 (Die1)	Die Enable Input .When #CEn is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
#CE1 (Die2)	
#CE2 (Die3)	
#CE3 (Die4)	
#CE4 (Die5)	
#CE5 (Die6)	
#CE6 (Die7)	
#CE7 (Die8)	
RDY/#BUSY	Ready busy.
#RES	Reset input.
#OE	Output enable.
#WE	Write Enable Input. Enables write operation.
VCC	Power supply, connect to 3.3V
VSS	Ground

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	-0.6 to +7.0	V
Input voltage relative to V _{SS}	V _{in}	-0.5 to +7.0	V
Operating temperature range	T _{OPR}	-55 to +125	°C
Storage temperature range	T _{STG}	-65 to +150	°C
Power Dissipation	P _D	1	W

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.3	3.6	V
	V _{SS}	0	0	0	V
Input voltage	V _{IL}	-0.3	-	0.8	V
	V _{IH}	1.9	-	V _{CC} +0.3	V
	V _H	V _{CC} -0.5	-	V _{CC} +1.0	V

5.3 DC Characteristics (V_{CC}=2.7 V to 3.6 V)

Table 4 DC characteristics

Parameter	Symbol	Test conditions	min.	max.	Unit
Output voltage low level	VOL	V _{CC} =2.7V , I _{OL} = 2.1mA	—	0.4	V
Output voltage high level	VOH	V _{CC} =2.7V , I _{OH} = -400uA	2.16	—	V

6 Typical Application

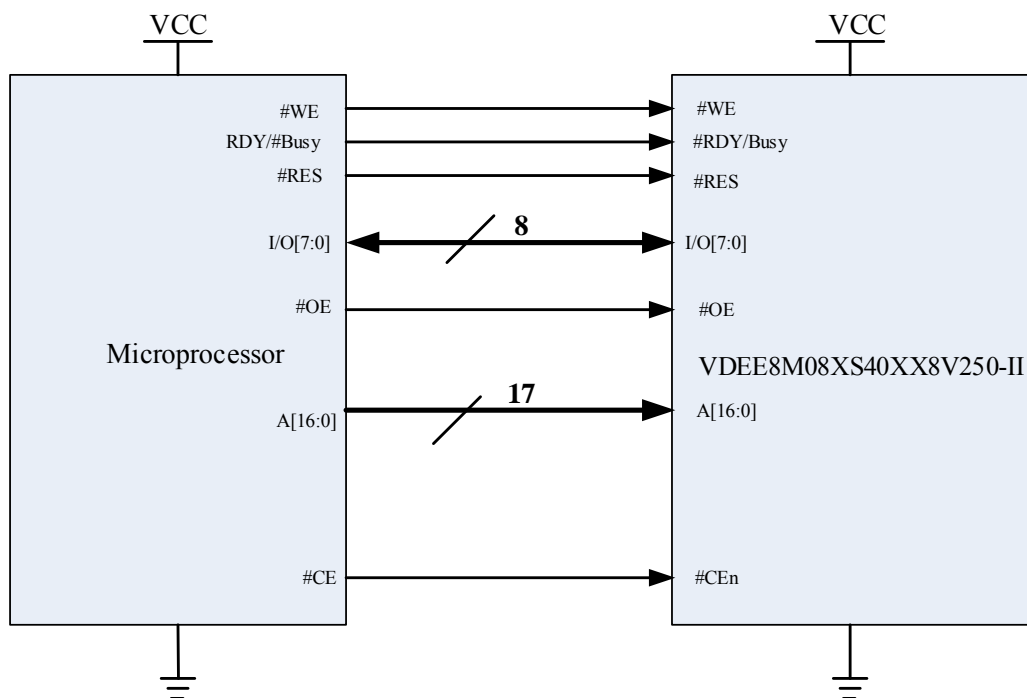


Figure 3 Typical application

7 Ordering Information

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>EE</u>	<u>8M</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>40</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>V</u>	<u>250</u>	<u>-II</u>
VDIC												
EEPROM												
Capability: 8M bit												
Bus Width: 8bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 40 Pin												
Temperature: E=0~+70℃;I=-40~+85℃;M=-55~+125℃												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer: 8layer												
Power Supply : 3.3V												
Speed: 250ns												
II=Second Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDEE8M08VS40EE8V250-II	8M	8	-	-	-	SOP40	0 ~ +70
VDEE8M08VS40IB8V250-II	8M	8	-	-	-	SOP40	-40 ~ +85
VDEE8M08VS40MM8V250-II	8M	8	-	-	-	SOP40	-55 ~ +125
VDEE8M08RS40MS8V250-II	8M	8	TBD	TBD	TBD	SOP40	-55 ~ +125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm2/mg)

³ SEU:SEU Threshold (Mev.cm2/mg)

8 Package Dimensions

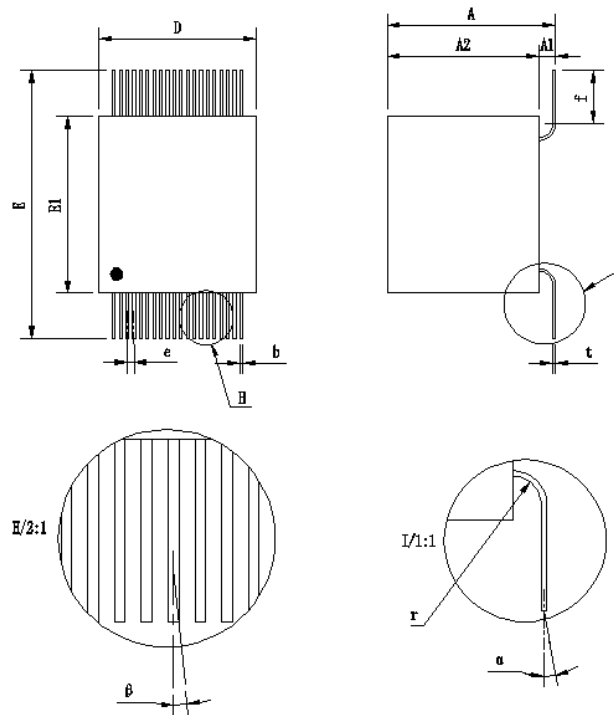


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	11.50	11.90
E	19.80	20.20
E1	13.00	13.40
f	3.98	
b	0.25	
e	0.50	
r	1.0	
t	0.20	
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	
NOTE : 1.Uint : mm 2. A1=A - A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Mar 27th,2020	First Created