VDIC
LOW-VOLTAGE
DIFFERENTIAL SIGNALING
RECEIVER

VDLV000108XS34XX1V01-32
USER MANUAL

Version: A0

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Contents

VDLV- Low-Voltage Differential Signal Receiver

3.3V Eight Line Receivers, Based on Quad

1 Description

The VDLV000108XS34XX1V01-32 is an eight CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The VDLV000108XS34XX1V01-32 accepts low voltage differential inputs signals and translates them to LVTTL/LVCMOS output levels.

The VDLV000108XS34XX1V01-32 provides a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

2 Features

- 400Mbps signaling rate
- Single 3.3V power supply
- -4 V to 5 V Common-Mode Input Voltage Range
- Integrated 110-Ω Line Termination Resistors On LVDT Products
- Active Failsafe Assures a High-Level Output With No Input
- Input Remains High-Impedance on Power Down
- Variable Temperature range

  0℃ to 70℃

  -40℃ to +85℃

  -55℃ to +125
- Available screening option for high reliability application

3 Block Diagram

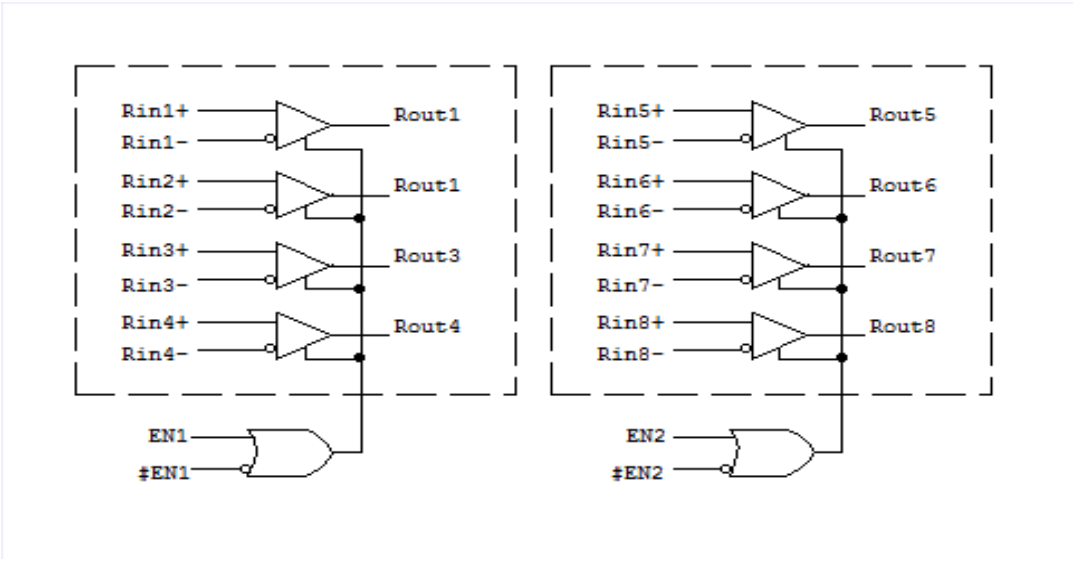

Figure 1 Block Diagram

4 Pin Descriptions

Pin ID	PIN #		Pin ID
Rin1-	1	18	Rin7-
Rin1+	2	19	Rin7+
Rout1	3	20	Rout7
EN1	4	21	#EN2
Rout2	5	22	Rout8
Rin2+	6	23	Rin8+
Rin2-	7	24	Rin8-
GND	8	25	VCC
GND	9	26	VCC
Rin5-	10	27	Rin3-
Rin5+	11	28	Rin3+
Rout5	12	29	Rout3
EN2	13	30	#EN1
Rout6	14	31	Rout4
Rin6+	15	32	Rin4+
Rin6-	16	33	Rin4-
GND	17	34	VCC

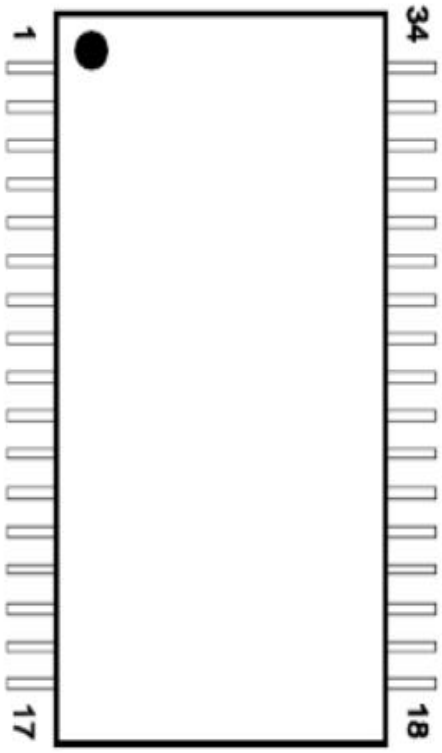

Figure 2 Pin Configuration

Table 1 Pin Description

Pin Name	Function
EN1 ~ EN2	Enable(HI=ENABLE)
#EN1 ~ #EN2	Enable(LO=ENABLE)
Rin1+ ~Rin8+	Differential(LVDS) non-inverting input
Rin1- ~ Rin8-	Differential(LVDS) inverting input
Rout1 ~ Rout8	LVTTL output signal
V_{CC}	Supply Voltage(3.0-3.6V)
GND	Ground

5 Electrical Specifications

5.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Supply Voltage	V_{DD}	-0.5 ~ +4.0	V
Input Voltage(EN, EN#, Rout)	V_{IN}	-1 ~ +6	
Input Voltage(Rin+, Rin-)		-5 ~ +6	
|Rin+ - Rin-|		1	
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	

5.2. Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

Parameter	Symbol	Min	TYP	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	——	5	V
Input Low Voltage	V_{IL}	0	——	0.8	V
Differential Voltage Input	$\|V_{ID}\|$	0	——	0.8	V
Common Mode Voltage Input	V_{IC}	-4	—	5	V

5.3. DC Characteristics

Table 4 DC Characteristics

Parameter	Symbol	Min	Max	Unit
Magnitude of differential input voltage	$\|V_{ID}\|$	——	0.8	V
Voltage at any bus terminal (separately or common-mode)	V_I or V_{IC}	-4	5	V

6 Typical Application

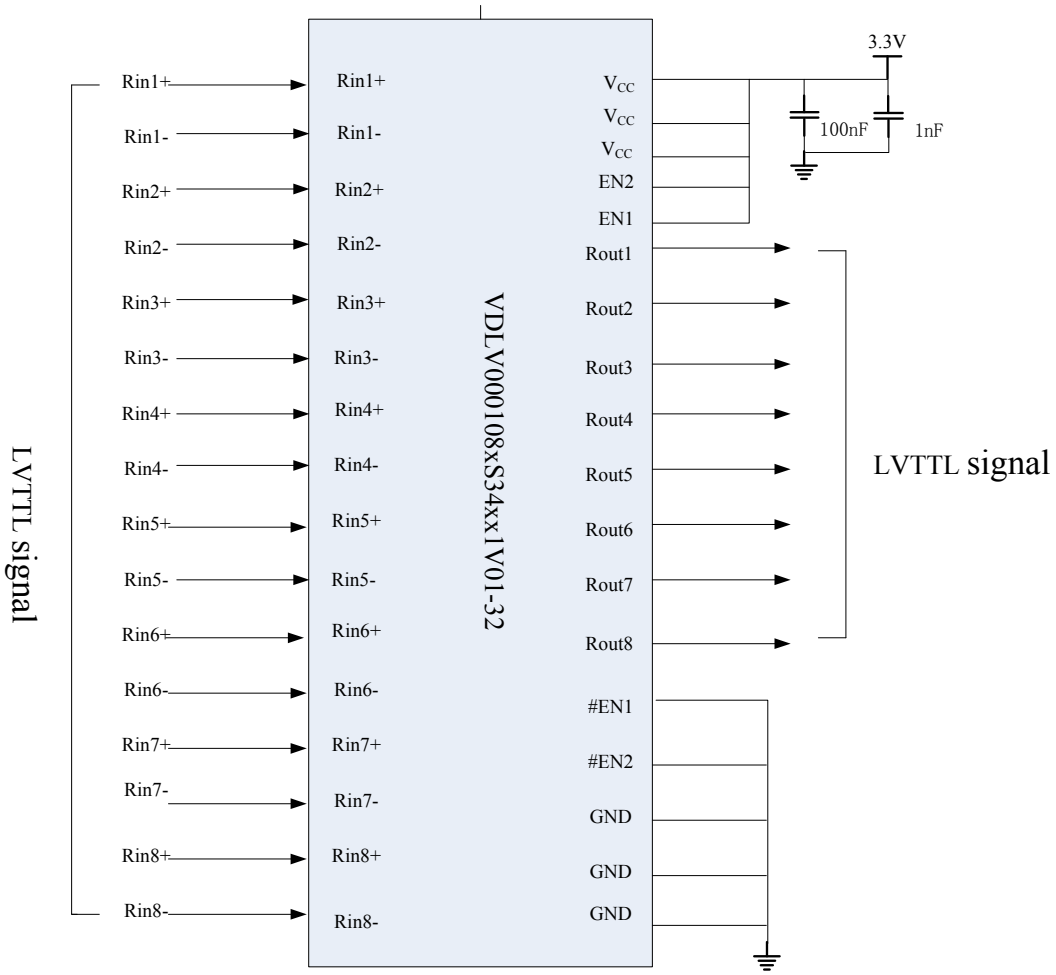

Figure 3 Typical Application

7 Ordering Information

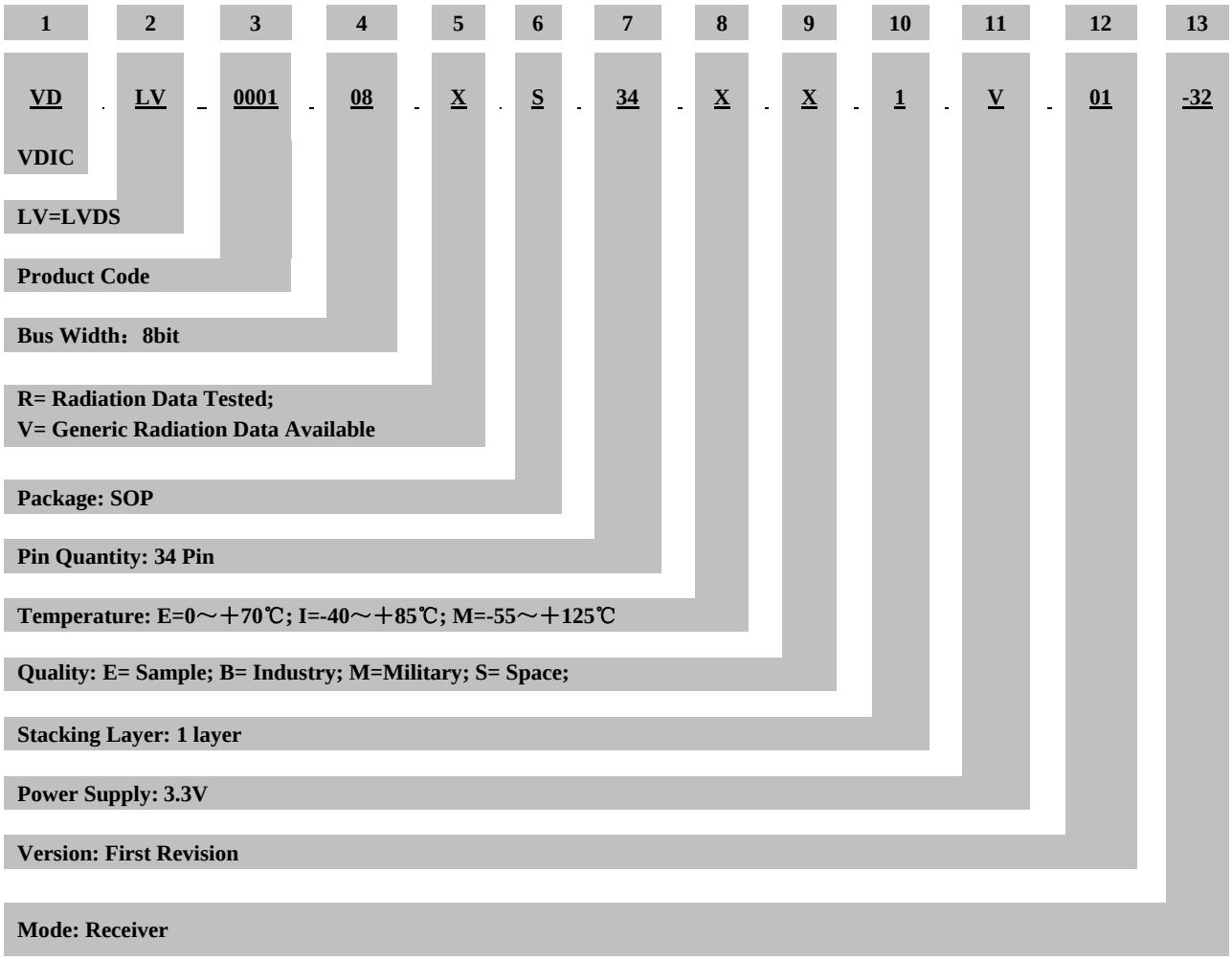

Table 5 Ordering Information

Bank Number	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
		TID[1]	SEL[2]	SEU[3]		
VDLV000108VS34EE1V01-32	08	--			SOP34	0 ~ + 70
VDLV000108VS34IB1V01-32	08	--			SOP34	-40 ~ + 85
VDLV000108VS34MM1V01-32	08				SOP34	-55～＋125℃
VDLV000108RS34MS1V01-32	08	100（TBD，25℃）	80（TBD，25℃）	5（TBD，25℃）	SOP34	-55～＋125℃

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（MeV.cm^2/mg）
[3] SEU:SEU Threshold （MeV.cm^2/mg）

8 Package Dimensions

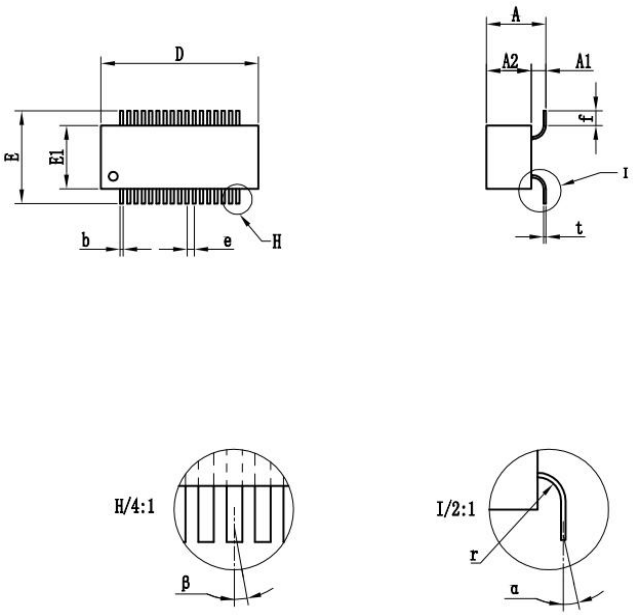

Figure 4 Package Dimensions

Table 6 Dimensions Information

	Min	Max
A	3.7	4.4
A2	2.5	3.1
D	13.9	14.3
E	7.8	8.2
E1	5.3	5.7
f	1.30	
b	0.3	
e	0.65	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1. Unit：mm 2. A1= A - A2		

9 Pads Designation

It is highly recommended to design pads as below.

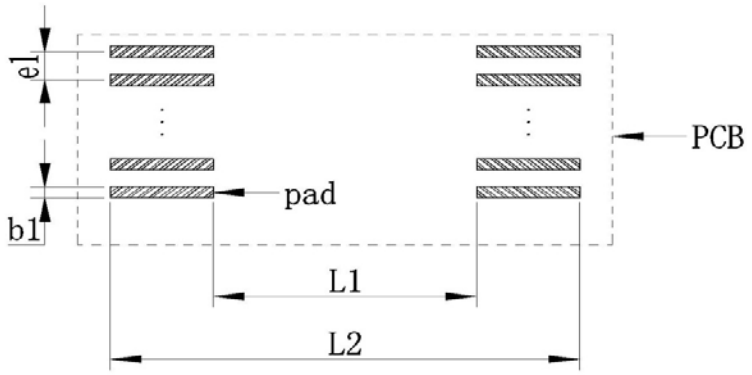

Figure 5 Pads Dimensions

NOTE:

e1: 0.65 mm;

b1: 0.45 mm;

L1: 2.2 mm;

L2: 9.2 mm.

10 Revision History

Table 7 Revision History

Revision	Date	Description
A0	Jul. 3, 2021	Initial Release